integrated circuit device, such as a smart card. In particular, as explained on pages 1 and 2 of the present specification, such devices include logic gates that draw current whenever their transistors change from a conductive state to a non-conductive state, or vice versa. It is possible to obtain an electrical signature representative of the activity of the integrated circuit device by monitoring the current as a function of time. Such a signature can enable a person to gain unauthorized access to the information stored in the device.

The present invention overcomes this vulnerability by effecting a change in the address bus lines and the data bus lines that are coupled to the gates. Specifically, at least one particular line from the address bus lines and the data bus lines is associated with an additional line. The signals on the particular line and the signal on the associated line are related by virtue of being complementary to each other. Thus, to summarize, key aspects of the present invention are as follows:

1. The invention applies to the address bus lines and the data bus lines of an integrated circuit device,
2. at least one of these bus lines is provided with an associated, additional line, and
3. the at least one line and its associated additional line convey signals that are complementary to each other.

In his stated rejection of the claims, the Examiner concedes that "Itoh does not specifically disclose wherein at least one line from the address bus lines and the data bus lines is associated with an additional line for conveying bits that are complementary to the bit conveyed over the at least one line".

Nevertheless, the claims have been rejected because of the Examiner's contention that "Kowalski discloses wherein at least one line from the address bus lines and the data bus lines is associated with an additional line for conveying bits that are complementary to the bit conveyed over the at least one line (see column 3, lines 43-50)."

However, it is respectfully submitted that the Examiner's description of Kowalski is in error. Although Kowalski, like the present invention, is directed to a technique aimed at preventing unauthorized access to information contained in a memory card, Kowalski focuses on the circuitry that is used to amplify the signal inputted to the memory card, not on the address and data bus lines. In column 1, lines 62-66, Kowalski points out that the electrical power used in such circuitry is low and, therefore, it must be amplified so that it can be transmitted properly to its intended destination. However, the amplifiers that are used for this purpose have a disadvantage in that "the current that flows through this amplifier thus reveals the logic state read by its value." See column 2, lines 11-12. In order to overcome this shortcoming, Kowalski's approach is to provide a detector provided with two detecting circuits which are parallel

connected with each other and that operate in a complementary way. The signals CHEPR and PRECH which are mentioned in the portion of Kowalski pointed out by the Examiner are used to control the two detectors 4, 5. However, neither of these signals is an address bus line or a data bus line. Kowalski explicitly states that the address signal is ADR and the data line is BLi. See column 3, lines 62-63. Kowalski does not modify the address and data buses in any way to achieve his objective of preventing unauthorized access. Consequently, Kowalski does not disclose, teach or even hint at the applicant's disclosed and claimed invention which adds an associated line to at least one of the address and data bus lines, as explained above.

The above-discussed distinction between the present invention and the applied references, particularly Kowalski, is explicitly recited in claim 1. More specifically, claim 1 explicitly recites address bus lines and data bus lines, and that "at least one line from the address bus lines and the data bus lines is associated with an additional line for conveying bits that are complementary to the bits conveyed over said at least one line." Accordingly, claim 1 is clearly and patentably distinguishable over the applied references.

Claims 2 and 6 are dependent from claim 1 and, thus, are allowable therewith.

The Examiner's indication of allowability with regard to claims 3-5 is acknowledged with appreciation.

Based on all of the above, it is respectfully submitted that the present application is now in proper condition for allowance. Prompt and favorable action to this effect and early passing of this application to issue are respectfully solicited.

Should the Examiner have any questions, comments, suggestions, or objections, he is invited to telephone the undersigned in order to facilitate the prosecution of this application by resolving any outstanding matters.

Respectfully submitted,

Thomas Langer

Thomas Langer
Reg. No. 27,264

Frishauf, Holtz, Goodman, Langer & Chick, P.C.
767 Third Avenue
New York, NY 10017-2023
Tel: (212) 319-4900
Fax: (212) 319-5101

TL/jh